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## DECLARATION

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I, Ryoichi Takaoka, of SHIGA INTERNATIONAL PATENT OFFICE, 2-3-1, Yaesu, Chuo-ku, Tokyo, Japan, understand both English and Japanese, am the translator of the English document attached, and do hereby declare and state that the attached English document contains an accurate translation of the official certified copy of Japanese Patent Application No. Hei 9-359899 and that all statements made herein are true to the best of my knowledge.

Declared in Tokyo, Japan

This 26th day of May, 2004

Ryoichi Takaoka



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[Document Type]

SPECIFICATION

[Title of the Invention] FRAME-RELAY FRAME TRANSMISSION CIRCUIT

[Claims]

1. A frame-relay frame transmission circuit wherein, when a received frame-relay frame is written in a memory, said frame is written from an address shifted from the top of a frame buffer.
2. A frame-relay frame transmission circuit according to claim 1, wherein the shift size is determined for each connection.

[Detailed Description of the Invention]

[0001]

[Technical Field]

The present invention relates to a frame-relay frame transmission circuit using a DMA transmission process, and in particular, to a frame-relay frame transmission circuit for converting a frame-relay frame into an AAL5 (ATM Adaptation Layer type 5) frame.

[0002]

[Background Art]

Fig. 1 shows a system for converting a received frame-relay frame into an ATM cell using a device performing a conventional direct memory access (DMA).

[0003]

A processor 105 performs a process through a processor bus 106 according to an instruction from software. When receiving a frame-relay frame through a channel, a frame receiver 101 in a frame transmission processing device 102 searches for (hunts) a frame buffer. A data FIFO block 103 temporarily stores frame data. A processor bus interface 104 transmits the frame to the searched frame buffer in a memory 107 through the DMA.

[0004]

A segmentation and reassembly (SAR) device 108 receives frame cell conversion information according to an instruction from the processor, and performs segmentation of the frame into an ATM cell.

[0005]

The memory 107 is accessed by the processor 105 and the frame transmission processing device 102, and stores the frame cell conversion information 109 for conversion of the frame into an ATM cell and data 110 of the frame in the frame buffer as shown in Fig. 2.

[0006]

The operation of the system will be explained. The processor 105 prepares an available frame buffer area in the frame transmission processing device 102. When starting to receive the frame receiver 101, the frame receiver 101 searched for the frame buffer and notifies the processor bus interface 104 of the top address of the frame buffer. The processor bus interface 104 transmits the received frame from the data FIFO block 103 to the memory 107 through the DMA according to the received address. At that time, the transmitted frame is

stored in the frame transmission processing device 102. After completion of the transmission, an interrupt notification is sent to the processor 105.

[0007]

By the software detecting the interrupt, the transmitted frame information is read from the frame transmission processing device 102. A multiprotocol section for the frame-relay frame which is written in the memory 107 is converted into a multiprotocol for ATM Adaptation Layer 5 (AAL5). While an area of an identifier for making a packet (capsuling) and transmitting the multiprotocol is assigned at the top of user data in the frame-relay frame and at the top of the AAL5 frame, the size of the area of the AAL5 frame is greater than the other kinds of protocols. To perform conversion between such protocols, the frame-relay frame is copied into a free area, which is not occupied by the frame data 11, in the memory 107 by the software, and the conversion of the protocols is performed. After completion of the conversion, the processor transfers the frame cell conversion information to the SAR device 108, which converts the frame into the AAL5 frame and produces an ATM cell.

[0008]

[Problem to be Solved by the Invention]

However, there is the problem that the frame transmission processing device 102 may write the frame data from the top of the searched frame buffer. When the area for the multiprotocol of the AAL5 frame is greater than that of the frame-relay frame, the frame-relay frame must be copied into a free area, which is not occupied by the frame data 11, in the memory 107 by software for performing conversion between such protocols, increasing the overhead caused by the

conversion process.

[0009]

This is because the conventional frame transmission processing device 102 is not designed according to concepts in which the frame is lengthened due to the conversion of the transmitted frame data and in which the top of the frame is converted.

[0010]

[Means for Solving the Problem]

The frame-relay frame transmission circuit of the present invention performs retrieval in a connection table preset by software before searching a frame buffer in which the received frame is to be written, obtains the shift size by which the frame is to be shifted from the top address of a frame buffer, and transmits the received frame-relay frame to the frame buffer by the DMA transmission process. In the conversion into a multiprotocol of the AAL5 frame, it is unnecessary to copy the frame-relay frame, which was written in a memory through a frame transmission processing device, into another area excluding a memory table for the frame data.

[0011]

[Modes for Carrying Out the Invention]

Referring to figures, the embodiment of the present invention will be explained. Fig. 3 is a schematic diagram showing a system of the present invention, Fig. 4 shows a memory 16 in detail, and Fig. 5 shows an example of a received frame which is shifted and written from the top of a searched (hunted) frame buffer.

[0012]

According to an instruction from a software, a processor 14 writes a set of a data link connection identifier (DLCI) and shift information for each reception channel to a memory table A18 which is a connection table. The DLCI is a connection identifier for frame-relay frame, and the shift information indicates how many bytes the received frame is to be shifted by from the top of the frame buffer. The size of the whole frame buffer and the start address are indicated to a frame transmission processing device 11.

[0013]

When receiving the top portion of the frame-relay frame from the channel, a frame receiver 10 in the frame transmission processing device 11 performs retrieval in the memory table A18 using the DLCI at the top portion as a key, and obtains the number of the bytes of the shift. The frame receiver 10 searches for (hunts) a frame buffer 21 and instructs a processor bus interface 13 to transmit the frame. An address indicated in the instruction is a shifted top address 22 of the frame buffer which was shifted by a given number of bytes.

[0014]

According to the indicated top address, the processor bus interface 13 receives the frame from a data FIFO block 12 and transmits it to a memory 16 through a DMA process.

[0015]

The transmitted frame information is stored in the frame transmission processing device 11. After the transmission is completed, the processor 14 transmits an interrupt notification to the processor 14. Through the software

detecting the interrupt, the transmitted frame information is read from the frame transmission processing device 11. A multiprotocol of the frame-relay frame written in the memory 107 is converted into an AAL5 multiprotocol. After conversion, the processor transfers frame cell conversion information in the memory table 19 to a SAR device 17, which converts (reassembles) the frame into the AAL5 frame and produces an ATM cell.

[0016]

#### [Effects of the Invention]

The first advantage of such a circuit is that, even when a multiprotocol of a frame-relay frame is converted into a multiprotocol of the AAL5 frame, it is unnecessary to copy the frame-relay frame, which was written in a memory through a frame transmission processing device, into another area excluding a memory table for the frame data.

[0017]

This is because the frame is written from a position which is shifted from the top of a searched frame buffer when the frame transmission processing device 11 writes the frame into the memory.

[0018]

The second advantage is that the waste of resources due to shifting of all frames can be avoided because a frame which does not need to be shifted is not shifted.

[0019]

This is because the shift size is determined for each connection.

### [Brief Description of the Drawings]

Fig. 1 is a schematic diagram showing a conventional frame transmission processing device and peripheral devices.

Fig. 2 is a diagram showing a memory in the conventional device of Fig. 1.

Fig. 3 is a schematic diagram showing a frame transmission processing device and peripheral devices of the present invention.

Fig. 4 is a diagram showing a memory in the device of Fig. 3.

Fig. 5 is a diagram showing an example of a frame which is written from a position shifted from the top of a frame buffer.

### [Brief Description of the Reference Symbols]

- 10 frame receiver
- 11 frame transmission device
- 12 data FIFO block
- 13 processor bus interface
- 14 processor
- 15 processor bus
- 16 memory
- 17 SAR device
- 18 to 20 memory table
- 20, 21 buffer top address